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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,527	BEREZIN ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *17-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-16* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10 April 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Restriction

1. Applicant's election without traverse of claims 1-16 in the reply filed on June 21, 2004 is acknowledged.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the reference character "212" (Figure 2) not mentioned in the description. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to because Figure 3 is not included in the "Brief Description of the Drawings" section. Appropriate correction is required.

Claim Objections

4. Claims 6, 10, and 16 are objected to as failing to comply with 37 CFR 1.75(a) for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitations "said first bias source" and "said second bias source" on lines 2-4. There is insufficient antecedent basis for these limitations in the claim. For examination purposes, the claim will be treated as if it reads, "said first bias line" and "said second bias line".

Claim 10 recites the limitation "said pixels" on lines 2 and 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 16 recites the limitation "the columns" on line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites a photoreceptor, a follower transistor connected to the photoreceptor, and a select transistor connected to the photoreceptor. The specification, however, does not disclose a select transistor connected to a photoreceptor. Rather, every embodiment discloses a select transistor connected to a follower transistor. The claim will be treated as if it reads as such.

Claims 2-9 are rejected because they are dependent on claim 1.

Claim 10 recites an array of photosensors including a photoreceptor, an in-pixel follower transistor, and a select line connected to the follower transistor. The specification, however, does not disclose a select line connected to a follower transistor. Rather, every embodiment discloses a select *transistor* connected to a follower transistor. The claim will be treated as if it reads as such.

Claims 11-13 are rejected because they are dependent on claim 10.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Merrill (U.S. Patent No. 6,211,510).

Regarding **claim 1**, Merrill discloses an image sensor, comprising:

a plurality of units (Figure 3A), each unit associated with accepting a pixel of an image, and each unit having a photoreceptor (photodiode 12) therein, a follower transistor (16; column 6, lines 56-57), connected to said photoreceptor, a select transistor (readout transistor 18; column 5, lines 2-3) connected to said follower transistor, and a reset transistor (14; column 5, lines 8-9) which controls applying a reset level;

a first bias line (V_d; column 2, lines 3-4) providing power to at least one of said transistors for a first unit (readout transistor 16), and a second bias line (V_{CC}; column 2, lines 4-6) providing power to another of said transistors (reset transistor 14), different than said one of said transistors of said first unit, such that said one and said another transistors are separately powered by separate bias lines.

Regarding **claim 2**, Merrill discloses:

said first bias line powers the follower transistor (V_d and readout transistor 16; column 2, lines 3-4) and said second bias line powers a reset transistor (V_{CC} and reset transistor 14; column 2, lines 4-6).

Regarding **claim 3,** Merrill discloses:

said photoreceptor is a photodiode (photodiode 12; column 1, line 64).

Regarding **claim 5,** Merrill discloses:

said sensor is an active pixel sensor (see title), formed of transistors which are compatible with CMOS techniques (column 1, lines 60-63), and each of a plurality of pixels of which includes an in-pixel follower transistor (16; column 6, lines 56-57), an in-pixel selection transistor (readout transistor 18; column 5, lines 2-3), and an in-pixel reset transistor (14; column 5, lines 8-9).

9. Claims 1-4 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuroda (U.S. Patent No. 6,512,543).

Regarding **claim 1**, Kuroda discloses an image sensor, comprising:

a plurality of units (Figure 4, comprised of multiple pixels 32), each unit associated with accepting a pixel of an image, and each unit having a photoreceptor (photoelectric conversion/storage section 33; column 6, line 21) therein, a follower transistor (driving transistor 35; column 6, lines 57-58), connected to said photoreceptor, a select transistor (selected-row transistor 42; column 9, lines 50-51) connected to said follower transistor, and a reset transistor (80; column 9, lines 19-20) which controls applying a reset level;

a first bias line (the unlabeled horizontal line connecting the pixels of the nth row in Figure 4) providing power to at least one of said transistors for a first unit, and a second bias line (line 79, connecting the pixels of the (n+1)th row in Figure 4 and reset

transistor 80 on the nth row) providing power to another of said transistors (reset transistor 80), different than said one of said transistors of said first unit, such that said one and said another transistors are separately powered by separate bias lines.

Regarding **claim 2**, Kuroda discloses:

said first bias line powers the follower transistor (unlabeled on the nth row in Figure 4) and said second bias line powers a reset transistor (80).

Regarding **claim 3,** Kuroda discloses:

said photoreceptor is a photodiode (see symbol in Figure 4 for photoelectric conversion/storage section 33).

Regarding **claim 4,** Kuroda discloses:

said photodiode is connected to a follower transistor for a first unit, and connected to be reset by a reset transistor of a second unit (see Figure 4, wherein reset transistor 80 is triggered by line 79 of the adjacent row).

Regarding **claim 10,** Kuroda discloses an active pixel sensor comprising:

an array of photosensors (Figure 4, comprised of multiple pixels 32), each element of the array including a photoreceptor (photoelectric conversion/storage section 33; column 6, line 21), an in-pixel follower (driving transistor 35; column 6, lines 57-58) connected to an output of said photoreceptor, and a select transistor (selected-row transistor 42; column 9, lines 50-51) connected to said follower transistor;

a reset transistor (80; column 9, lines 19-20) connected to reset a level of charge produced by said photoreceptor; and

a pair of biasing connections including a first biasing connection (line 79, connecting the pixels of the (n+1)th row in Figure 4 and reset transistor 80 on the nth row) connected to said reset transistor, and a second biasing connection (the unlabeled horizontal line connecting the pixels of the nth row in Figure 4), separated from said first biasing connection, connected to said follower.

Regarding **claim 11,** Kuroda discloses:

said photoreceptor is connected between a reset transistor of a first line, and a follower of a second line different than said first line (see Figure 4, wherein reset transistor 80 is triggered by line 79 of the adjacent row).

Regarding **claim 12,** Kuroda discloses:

a dynamic mode read out transistor (selected row driving transistor 40; column 9, line 41), associated with at least one of said biasing connections, and allowing said biasing connection to be active for only a part, but not all, of a period (see chart 66 in Figure 5; column 9, lines 36-38).

10. Claims 1, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill (U.S. Patent No. 5,614,744).

Regarding **claim 1**, Merrill discloses an image sensor (shown in Figure 1A), comprising:

a plurality of units (including a "column of pixels"; column 1, lines 54-55), each unit associated with accepting a pixel of an image, and each unit having a photoreceptor therein (photogate PG; column 1, line 50), a follower transistor (column 1, line 53), connected to said photoreceptor, a select transistor (row selection transistor Q; column 1,

lines 53-54) connected to said follower transistor, and a reset transistor (transistor R; column 1, line 52) which controls applying a reset level;

a first bias line (VDD) providing power to at least one of said transistors for a first unit, and a second bias line (X) providing power to another of said transistors, different than said one of said transistors of said first unit, such that said one and said another transistors are separately powered by separate bias lines.

Regarding **claim 8**, Merrill discloses (shown in Figure 1A):

said photoreceptor is a photogate (column 1, line 50), and further comprising a floating diffusion portion (node FD; column 1, line 51) in the substrate connected to said follower transistor, and further comprising a transfer gate (TX; column 1, line 51), coupled between said photogate and said floating diffusion, which is activated to allow charge in said photogate to dump into said floating diffusion (column 2, lines 11-13).

Regarding **claim 9**, Merrill discloses (shown in Figure 1A):

a reset diffusion (unlabeled and shown to the right of reset transistor R and connected to VDD) storing a reset level (VDD), and wherein said reset transistor is connected between said floating diffusion and said reset level.

11. Claims 14, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Okamoto (U.S. Patent No. 6,580,063).

Regarding **claim 14**, Okamoto discloses:

an array of pixels (Figure 8), each pixel including a photosensor (801), and at least first (803) and second transistors (804) associated with said photosensor in said each

pixel, said first transistor connected to receive power from a first power supply source (807) over a first line, and said second transistor connected to receive power from a second power supply source (805) over a second line totally separate from said first power supply line.

Regarding **claim 15**, Okamoto discloses:

said first transistor and said second transistor have drains which are not electrically connected (as stated in column 1, lines 35-36, the drain of transistor 803 is connected to power supply line 807).

Regarding **claim 16,** Okamoto discloses:

a steady state current generator (current source 809; column 1, lines 37-38), providing a first, "on" mode connecting the columns to ground (column 1, lines 37-43) and a second "off" mode which provides floating columns (activation of bias line 815 occurs at a specific time during the operation, as stated in column 2, lines 11-19; it is therefore inherent that a time exists when the line is inactive and the columns are floating).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 6,211,510) in view of Andoh (U.S. Patent No. 5,539,461).

Claim 6 may be treated like claim 5. However, Merrill is silent with regard to connecting the select and reset transistors to a first bias source and connecting the follower transistor to a second bias source.

Andoh discloses the image sensor in Figure 4, wherein:

> said select and reset transistors are connected to said first bias source (line VS-2 is a first bias source, and reset transistor 43a is connected to the line in addition to the unlabeled select transistor, corresponding to transistor 33, in the row above the labeled transistors) and said follower transistors (32) connected to said second bias source (line VL-1).

As stated in column 6, lines 57-59, an advantage to this configuration is that selection and reset of rows of pixels may be combined into a single operation. This simplifies the operation of

the circuit. For this reason, it would have been obvious to one of ordinary skill in the art for Merrill's sensor to combine row operations, such as in the way described by Andoh.

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Miyawaki (U.S. Patent Application Publication No. 2002/0001037).

Claim 13 may be treated like claim 10. However, Kuroda is silent with regard to referencing pixels to a ground reference and then floating the pixels.

Miywaki discloses the image sensor shown in Figure 5, wherein:

> a connection (7) is activated to cause said pixels (S) to be referenced to a ground reference (paragraph 0130), and is opened to cause said pixels to be floated (paragraph 0130).

An advantage to grounding and removing pixels is that accumulated charge on a column output line may be removed, thus reducing noise. For this reason, it would have been obvious to one of ordinary skill in the art to have Kuroda's sensor ground and float a pixel connection line.

Allowable Subject Matter

16. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art could be located that teaches or fairly suggests an active pixel sensor with each pixel containing a follower transistor, a select transistor, and a reset transistor, wherein a

second bias source is connected commonly to a plurality of followers in a first row and reset transistors in a second row.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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September 25, 2004

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